The following listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A reader of an RFID system comprising:

excitation circuitry for generating a higher voltage excitation signal;

receiving circuitry for reading a lower voltage transponder signal;

an antenna coupled with said excitation circuitry for transmitting said excitation signal and coupled with said receiving circuitry for receiving said transponder signal; and

a low voltage signal stripping circuit included in said receiving circuitry coupled with said antenna for isolating said transponder signal from said excitation signal preliminary to said receiving circuitry reading said transponder signal, said low voltage signal stripping circuit comprising an inlet resistor, an amplifier, a feedback circuit and a DC shift voltage or a DC shift current source, wherein said feedback circuit has a first pathway including a first pair of clamping diodes aligned in series in a first direction, a second pathway including a second pair of clamping diodes aligned in series in a second direction opposite said first direction, and a third pathway including a feedback resistor having a resistance.

Claim 2 (original): The reader of claim 1, wherein said inlet resistor is positioned in series between said antenna and said amplifier.

Claim 3 (currently amended): The reader of claim ~~1~~ 7, wherein said feedback circuit has a pathway including a pair of clamping diodes aligned in series.

Claim 4 (currently amended): The reader of claim ~~1~~ 7, wherein said feedback circuit has a pathway including a feedback resistor having a resistance.

Claim 5 (currently amended): The reader of claim ~~4~~ 1, wherein said inlet resistor has a resistance about equal to said resistance of said feedback resistor.

Claim 6 is canceled without prejudice.

Claim 7 (currently amended): A reader of an RFID system comprising:

excitation circuitry for generating a higher voltage excitation signal;

receiving circuitry for reading a lower voltage transponder signal;

an antenna coupled with said excitation circuitry for transmitting said excitation signal and coupled with said receiving circuitry for receiving said transponder signal; and

a low voltage signal stripping circuit included in said receiving circuitry coupled with said antenna for isolating said transponder signal from said excitation signal preliminary to said receiving circuitry reading said transponder signal, said low voltage signal stripping circuit comprising an inlet resistor, an amplifier, a feedback circuit and a DC shift voltage or a DC shift current source ~~The reader of claim 1~~, wherein said inlet resistor is a high voltage component and said amplifier and said feedback circuit are low voltage components.

Claim 8 (original): The reader of claim 1, wherein said amplifier and said feedback circuit are included in an application specific integrated circuit.

Claim 9 (currently amended): A reader of an RFID system comprising:

excitation circuitry for generating a higher voltage excitation signal;

receiving circuitry for reading a lower voltage transponder signal;

an antenna coupled with said excitation circuitry for transmitting said excitation signal and coupled with said receiving circuitry for receiving said transponder signal;

a low voltage signal stripping circuit included in said receiving circuitry coupled with said antenna for isolating said transponder signal from said excitation signal preliminary to said receiving circuitry reading said transponder signal, said low voltage signal stripping circuit comprising an inlet resistor, an amplifier, a feedback circuit and a DC shift voltage or a DC shift current source; and ~~The reader of claim 1, further comprising~~

a summing node positioned upstream of said amplifier and downstream of said inlet resistor, said feedback circuit and said DC shift voltage or said DC shift current source to sum outputs from said inlet resistor, said feedback circuit and said DC shift voltage or said DC shift current source.

Claim 10 (original): The reader of claim 1, wherein said amplifier has a first input coupled with said inlet resistor and a second input tied to a reference voltage.

Claim 11 (original): The reader of claim 10, wherein said first input of said amplifier is an inverting negative input.

Claim 12 (original): The reader of claim 10, wherein said second input of said amplifier is a non-inverting positive input.

Claim 13 (currently amended): A reader of an RFID system comprising:

excitation circuitry for generating a higher voltage excitation signal;

receiving circuitry for reading a lower voltage transponder signal;

an antenna coupled with said excitation circuitry for transmitting said excitation signal and coupled with said receiving circuitry for receiving said transponder signal;

a low voltage signal stripping circuit included in said receiving circuitry coupled with said antenna for isolating said transponder signal from said excitation signal preliminary to said receiving circuitry reading said transponder signal, said low voltage signal stripping circuit comprising an inlet resistor, an amplifier, a feedback circuit and a DC shift voltage or a DC shift current source; and

a summing node positioned upstream of said amplifier and downstream of said inlet resistor, said feedback circuit and said DC shift voltage or said DC shift current source to sum outputs from said inlet resistor, said feedback circuit and said DC shift voltage or said DC shift current source ~~The reader of claim 9~~, wherein said amplifier has a first input coupled with said summing node and a second input tied to a reference voltage.

Claim 14 (original): The reader of claim 13, wherein said first input of said amplifier is an inverting negative input.

Claim 15 (original): The reader of claim 13, wherein said second input of said amplifier is a non-inverting positive input.

Claims 16-45 are canceled without prejudice.

Claim 46 (new): The reader of claim 7, wherein said inlet resistor is positioned in series between said antenna and said amplifier.

Claim 47 (new): The reader of claim 7, wherein said feedback circuit has a first pathway including a first pair of clamping diodes aligned in series in a first direction, a

second pathway including a second pair of clamping diodes aligned in series in a second direction opposite said first direction, and a third pathway including a feedback resistor.

Claim 48 (new): The reader of claim 4, wherein said inlet resistor has a resistance about equal to said resistance of said feedback resistor.

Claim 49 (new): The reader of claim 7, wherein said amplifier and said feedback circuit are included in an application specific integrated circuit.

Claim 50 (new): The reader of claim 7, wherein said amplifier has a first input coupled with said inlet resistor and a second input tied to a reference voltage.

Claim 51 (new): The reader of claim 50, wherein said first input of said amplifier is an inverting negative input.

Claim 52 (new): The reader of claim 50, wherein said second input of said amplifier is a non-inverting positive input.

Claim 53 (new): The reader of claim 9, wherein said amplifier and said feedback circuit are included in an application specific integrated circuit.

Claim 54 (new): The reader of claim 9, wherein said inlet resistor is positioned in series between said antenna and said amplifier.

Claim 55 (new): The reader of claim 9, wherein said feedback circuit has a pathway including a pair of clamping diodes aligned in series.

Claim 56 (new): The reader of claim 9, wherein said feedback circuit has a pathway including a feedback resistor having a resistance.

Claim 57 (new): The reader of claim 56, wherein said inlet resistor has a resistance about equal to said resistance of said feedback resistor.

Claim 58 (new): The reader of claim 9, wherein said feedback circuit has a first pathway including a first pair of clamping diodes aligned in series in a first direction, a second pathway including a second pair of clamping diodes aligned in series in a second direction opposite said first direction, and a third pathway including a feedback resistor.

Claim 59 (new): The reader of claim 9, wherein said amplifier has a first input coupled with said inlet resistor and a second input tied to a reference voltage.

Claim 60 (new): The reader of claim 59, wherein said first input of said amplifier is an inverting negative input.

Claim 61 (new): The reader of claim 59, wherein said second input of said amplifier is a non-inverting positive input.

Claim 62 (new): The reader of claim 13, wherein said amplifier and said feedback circuit are included in an application specific integrated circuit.

Claim 63 (new): The reader of claim 13, wherein said inlet resistor is positioned in series between said antenna and said amplifier.

Claim 64 (new): The reader of claim 13, wherein said feedback circuit has a pathway including a pair of clamping diodes aligned in series.

Claim 65 (new): The reader of claim 13, wherein said feedback circuit has a pathway including a feedback resistor having a resistance.

Claim 66 (new): The reader of claim 65, wherein said inlet resistor has a resistance about equal to said resistance of said feedback resistor.

Claim 67 (new): The reader of claim 13, wherein said feedback circuit has a first pathway including a first pair of clamping diodes aligned in series in a first direction, a second pathway including a second pair of clamping diodes aligned in series in a second direction opposite said first direction, and a third pathway including a feedback resistor.